IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Patent Application of:	)	
Bunsho KURAMORI *et al.*	)	Group Art Unit: 2816
Serial No.: **10/670,773**	)	Examiner: Terry Lee Englund
Filed: **September 26, 2003**	)	Confirmation No. 4336
For: **SUBSTRATE VOLTAGE GENERATING CIRCUIT WITH IMPROVED LEVEL SHIFT CIRCUIT (AS AMENDED)**	)	Date: December 15, 2006

APPEAL BRIEF (AMENDED)

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The following amended Appeal Brief is submitted in support of the Notice of Appeal filed May 30, 2006, and in further response to the Notification of Non-Compliant Brief mailed November 17, 2006.

In the Amended Appeal Brief, Appellants amended Sections III and IV, Status of Claims and Amendments, respectively, to provide additional details of the Final Office and Advisory Actions and to discuss the Examiner's identification of a clerical error in Appellants' response to the Final Office mailed November 30, 2005, wherein the claim language of claim 3, at line 15, did not correspond to that recited in the Appellants' response to the Non-Final Office Action mailed September 12, 2005. Also, Appellants amended Section V, Summary of the Claimed Subject Matter to provide proper references to the independent and dependent claims. The original Appeal Brief did not provide the correct Title of the Invention, which was previously amended by the Appellants in their Response to the Final Office Action mailed November 5, 2005.

Based on the remarks presented herein, Appellants respectfully appeal the Examiner's final rejection of claims 1 – 10 of the above-identified application. In addition, Appellants respectfully request that the Board of Patent Appeals and Interferences reverse the final rejection of these claims.

I. REAL PARTY IN INTEREST

Oki Electric Industry Co., LTD. is the assignee and real party in interest.

II. RELATED APPEALS AND INTERFERENCES

There are presently no appeals or interferences known to the Appellants, the Appellants' representative, or the assignee, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Independent claims 7 and 9 are deemed as allowable, if rewritten or amended to satisfactorily overcome the rejection under 35 U.S.C. §112, 2nd paragraph, set forth in the Final Office Action of November 30, 2005.

For the purposes of this Appeal, claims 1 – 10 stand rejected. Thus, this Appeal is taken from the rejection of claims 1 – 10, as submitted in the Appendix herewith.

IV. STATUS OF AMENDMENTS

No amendment has been filed after the Final Office Action mailed November 30, 2005. In reply to the Final Office Action, Appellants submitted a response entitled "Amendment After Final," on May 30, 2006. The Examiner subsequently issued an Advisory Action on July 5, 2006, maintaining all rejections made in the Final Office Action. In addition, the Examiner, at page 3 of the Advisory Action, stated that "although not amended, claim 3 (line 15) does not correspond to the previous version of the claim (*i.e.*, the claim language recited in Appellants' response to the Non-Final Office Action dated September 12, 2005). In response to the Examiner's comment, Appellants respectfully submit that claim 3, at line 15, as presented in the May 30, 2006 response, does not recite the original phrase " a sixth transistor of the." Such omission is a clerical error and is

inadvertent. Appellants will file an Amendment After Appeal pursuant to 37 C.F.R. §41.33(b) to revert back to the claim language, as originally recited.

V. SUMMARY OF CLAIMED SUBJECT MATTER

This Appeal is taken from claims 1 – 10, of which claims 1, 7 and 9 are independent. It should be noted that references to particular elements in the following discussion are for illustrative purposes to benefit the Examiner's understanding of the claimed invention and not intended to unduly limit the scope of Appellants' claimed invention.

Independent Claim 1

With respect to independent claim 1, the present invention recited therein relates to a substrate voltage generating circuit comprising (1) a first power supply node (see *e.g.*, p. 2, l. 9) supplied with a first potential level (VDD) (*e.g.*, see p. 5, l. 16); (2) a second power supply node (see *e.g.*, p. 2, l. 20 – p. 3, ll. 1 – 2) supplied with a second potential level (VSS) (see *e.g.*, p. 5, l. 14) lower than the first potential level; (3) an output node (see *e.g.*, p. 3, ll. 2 – 3) (*e.g.*, OUT.vbb; (see *e.g.*, p. 4, l. 15)) having a third potential level (VBB) (see *e.g.*, p. 4, l. 16) lower than the second potential level; (4) a level shift circuit (see *e.g.*, p. 3, ll. 7 – 9) (see *e.g.*, 101, 102 at p. 4, l. 16 – p. 5, l. 5), which is coupled between the first power supply node and the output node, which receives an input signal having the first and second potential levels, and which outputs an output signal having the first potential level and the third potential level; and (5) a switch circuit (see *e.g.*, p. 3, ll. 7 – 9; *e.g.*, SW1 (p. 4, l. 18) and SW2 (p. 4, l. 20)), which connects the second power supply node to the output node in response to the output signal.

According to the specification, a first potential level is VDD, a second potential level is VSS, and a third potential level is VBB. VDD is disclosed in the specification as a high (H) potential level (see *e.g.*, p. 12, ll. 1 – 5), while VSS is a low (L) potential level (see *e.g.*, p. 11, l. 20) and VBB, which is the generated substrate voltage, has a potential that is lower than the second potential level VSS (see *e.g.*, p. 5, l. 20 – p. 6, l. 2). Support for the claimed features can be found at least in, *e.g.*, Fig. 1 and its description in the specification (see *e.g.*, p. 2, l. 18 – p. 9, l. 12).

Dependent Claim 2

With respect to dependent claim 2, which depends from claim 1, the claim further specifies that the level shift circuit comprises: (1) a first transistor (see *e.g.*, P1 of Fig. 2 and p. 9, l. 17) of a first conductivity type which has a gate receiving the input signal, a source connected to the first power supply node, and a drain (see *e.g.*, p. 9, l. 20 – p. 10, l. 2); (2) a second transistor (see *e.g.*, P2 of Fig. 2; and p. 9, l. 17) of the first conductivity type which has a gate receiving the input signal, a source connected to the first power supply node, and a drain coupled to the switch circuit (see *e.g.*, p. 10, ll. 3 – 7); (3) a third transistor (see *e.g.*, N1 of Fig. 2 and p. 9, l. 18) of a second conductivity type which has a gate connected to the gate of the first transistor, a source, a drain connected to the drain of the first transistor, and a gate oxide film having a first thickness (see *e.g.*, p. 10, ll. 7 – 9); (4) a fourth transistor (see *e.g.*, N2 of Fig. 2 and p. 9, l. 18) of the second conductivity type which has a gate connected to the gate of the second transistor, a source, a drain connected to the drain of the second transistor, and a gate oxide film having the first thickness (see *e.g.*, p. 10, ll. 9 – 12); (5) a fifth transistor (*e.g.*, N3 of Fig. 2; see p. 9, l. 19) of the second conductivity type which has a gate connected to the drain of the second transistor, a source connected to the output node, a drain connected to the source of the third transistor, and a gate oxide film having a second thickness thinner than the first thickness (p. 10, ll. 12 – 15); and (6) a sixth transistor (*e.g.*, N4 of Fig. 2; see p. 9, l. 19) of the second conductivity type which has a gate connected to the drain of the first transistor, a source connected to the output node, a drain connected to the source of the fourth transistor, and a gate oxide film having the second thickness (see *e.g.*, p. 10, ll. 15 – 17).

Support for the feature of claim 2 can be found in, *e.g.*, Fig. 2 and its associate description in the first preferred embodiment in the specification (see *e.g.*, p. 9, l. 13 – p. 16, l. 7). Support for the thickness of the gate oxide film of transistors N1 and N2 being thicker than those of transistors N3 and N4 can be found in the specification (see *e.g.*, p. 10, l. 19 – p. 11, l. 3; p. 12, l. 12 – 15; and p. 14, ll. 13 – 19).

Dependent Claim 3

With respect to dependent claim 3, which depends from claim 1, the claim further specifies that the level shift circuit comprises: (1) a first transistor (see *e.g.*, P31 of Fig. and p. 7, l. 1) of a first conductivity type which has a gate receiving the input signal, a source connected to the first power supply node, and a drain (see *e.g.*, p. 17, ll. 1 – 6); (2) a second transistor (see *e.g.*, P32 of Fig. 3 and p. 17, l. 1) of the first conductivity type which has a gate

receiving the input signal, a source connected to the first power supply node, and a drain coupled to the switch circuit (see *e.g.*, p. 17, ll. 7 – 11); (3) a third transistor (see *e.g.*, N31 of Fig. 3 and p. 17, l. 11) of a second conductivity type which has a gate connected to the drain of the second transistor, a source, a drain connected to the drain of the first transistor, and a gate oxide film having a first thickness (see *e.g.*, p. 17, ll. 11 – 13); (4) a fourth transistor (see *e.g.*, N32 of Fig. 3 and p. 17, l. 14) of the second conductivity type which has a gate connected to the drain of the first transistor, a source, a drain connected to the drain of the second transistor, and a gate oxide film having the first thickness (see *e.g.*, p. 17, ll. 14 – 16); (5) a fifth transistor (see *e.g.,* N33 of Fig. 3 and p. 17, l. 17) of the second conductivity type which has a gate connected to the gate of the first transistor, a source connected to the output node, a drain connected to the source of the third transistor, and a gate oxide film having a second thickness thicker than the first thickness (see *e.g.*, p. 17, ll. 16 – 19); and (6) a sixth transistor (see *e.g.*, N34 of Fig. 3 and p. 17, l. 19) of the second conductivity type which has a gate connected to the gate of the second transistor, a source connected to the output node, a drain connected to the source of the fourth transistor, and a gate oxide film having the second thickness (see *e.g.*, p. 17, l. 19 – p. 18, l. 3).

Support the features of claim 3 can be found in Fig. 3 and its description in the second preferred embodiment in the specification at pages 14 – 16. Support for the feature wherein the thickness of the gate oxide film of the 3rd and 4th transistors is greater than the gate oxide film of the 5th and 6th transistors can be found in, see *e.g.*, p. 18, ll. 4 – 8.

Dependent Claim 4

With respect to dependent claim 4, which depends from claim 1, the claim further specifies that the switch circuit comprises: (1) a switching element (see *e.g.*, SW1, SW2 in Fig. 1) which has a control electrode receiving the output signal, a first electrode connected to the second power supply node, and a second electrode connected to the output node (see *e.g.*, OUT.vbb in Fig. 1); and a capacitor (see *e.g.*, c1, c2 in Fig. 1) coupled between the first electrode and the control electrode (see *e.g.*, p. 4, l. 12 – p. 5, l. 5 and p 6, ll. 10 – 20).

Dependent Claim 5

With respect to dependent claim 5, which depends from claim 1, the claim further recites that the second potential level is 0 volt, as supported on p. 5, ll. 15 – 16, for example.

Dependent Claim 6

With respect to dependent claim 6, which depends from claim 1, the claim further recites that third potential level is a negative voltage level, as recited in the amended page 6, lines 1-2 of the specification.

Independent Claim 7

With respect to independent claim 7, the invention recited therein relates to a voltage level shifting circuit comprising: (1) a first transistor (see *e.g.*, P1 of Fig. 2 and p. 9, l. 17) of a first conductivity type which has a gate receiving an input signal, a source connected to a first supply node supplied with a first potential level, and a drain (see *e.g.*, p. 9, l. 19 – p. 10, l. 2); (2) a second transistor (see *e.g.*, P2 of Fig. 3 and p. 9, l. 17) of the first conductivity type which has a gate receiving the input signal, a source connected to the first supply node, and a drain coupled to an output node (see *e.g.*, OUT.101 of Fig. 2 and p. 5, ll. 6 – 8); (3) a third transistor (see *e.g.*, N1 of Fig. 2 and p. 9, l. 18) of a second conductivity type which has a gate connected to the gate of the first transistor, a source, a drain connected to the drain of the first transistor, and a gate oxide film having a first thickness (see *e.g.*, p. 10, ll. 6 – 9); (4) a fourth transistor (see *e.g.*, N2 of Fig. 2 and p. 9, ll. 18-19) of the second conductivity type which has a gate connected to the gate of the second transistor, a source, a drain connected to the drain of the second transistor, and a gate oxide film having the first thickness (see *e.g.*, p. 10, ll. 9 – 11); (5) a fifth transistor (see *e.g.*, N3 of Fig. 2 and p. 9, l. 19) of the second conductivity type which has a gate connected to the drain of the second transistor, a source connected to a second supply node supplied with a second potential level lower than the first potential level, a drain connected to the source of the third transistor, and a gate oxide film having a second thickness thinner than the first thickness (see *e.g.*, p. 10, ll. 12 – 15 and p. 10, l. 19 – p. 11, l. 3); and (6) a sixth transistor (see *e.g.*, N4 of Fig. 2 and p. 9, l. 19) of the second conductivity type which has a gate connected to the drain of the first transistor, a source connected to the second supply node, a drain connected to the source of the fourth transistor, and a gate oxide film having the second thickness (see *e.g.*, p. 10, ll. 15 – 16 and p. 10, l. 19 – p. 11, l. 3).

Support for claim 7 can be found at least in, *e.g.*, in Fig. 2 and its respective description in the specification. Support for the thickness of the gate oxide film of transistors N1 and N2 being thicker than those of transistors N3 and N4 can be found in the bridging paragraph between pages 10 – 11 of the specification .

Dependent Claim 8

With respect to dependent claim 8, which depends from claim 7, the claim further specifies the first potential level is a positive voltage level and the second potential level is a negative voltage level, as disclosed in original claim 8, which is part of the invention disclosure (see *e.g.*, p. 2, l. 19; p. 3, l. 3; and p. 5, ll. 15 – 16).

Independent Claim 9

With respect to independent claim 9, the invention recited therein relates to a voltage level shifting circuit comprising: (1) a first transistor (see *e.g.*, P31 of Fig. 3 and p. 17, l. 1) of a first conductivity type (see *e.g.*, p. 17, l. 4) which has a gate receiving an input signal, a source connected to a first supply node supplied with a first potential level, and a drain (see *e.g.*, p. 17, ll. 3 – 7); (2) a second transistor (see *e.g.*, P32 of Fig. 3 and p. 17, l. 1) of the first conductivity type (see *e.g.*, p. 17, l. 4) which has a gate receiving the input signal, a source connected to the first supply node, and a drain coupled to an output node (see *e.g.*, p. 17, ll. 7 – 11); (3) a third transistor (see *e.g.*, N31 of Fig. 3 and p. 17, l. 2) of a second conductivity type (see *e.g.*, p. 17, l. 8) which has a gate connected to the drain of the second transistor, a source, a drain connected to the drain of the first transistor (see *e.g.*, p. 17, ll. 11 – 13), and a gate oxide film having a first thickness (see *e.g.*, p. 18, ll. 4 – 8); (4) a fourth transistor (see *e.g.*, N32 of Fig. 3 and p. 17, l. 2)of the second conductivity type (see *e.g.*, p. 17, l. 8) which has a gate connected to the drain of the first transistor, a source, a drain connected to the drain of the second transistor (see *e.g.*, p. 17, ll. 14 – 16), and a gate oxide film having the first thickness (see *e.g.*, p. 18, ll. 4 – 8); (5) a fifth transistor (see *e.g.*, N33 of Fig. 3 and p. 17, l. 2) of the second conductivity type (see *e.g.*, p. 17, l. 8) which has a gate connected to the gate of the first transistor, a source connected to a second supply node supplied with a second potential level lower than the first potential level, a drain connected to the source of the third transistor (see *e.g.*, p. 17, ll. 16 – 19), and a gate oxide film having a second thickness thicker than the first thickness(see *e.g.*, p. 18, ll. 4 – 8); and (6) a sixth transistor (see *e.g.*, N34 of Fig. 3 and p. 17, l. 3) of the second conductivity type (see *e.g.*, p. 17, l. 8) which has a gate connected to the gate of the second transistor, a source connected to the second supply node, a drain connected to the source of the fourth transistor (see *e.g.*, p. 17, l. 19 – p. 18, l. 2), and a gate oxide film having the second thickness (see *e.g.*, p. 18, ll. 4 – 8).

Support for the claimed features can be found at least in Fig. 3 and its respective description in the specification. Support for the feature wherein the thickness of the gate

oxide film of the 3rd and 4th transistors is greater than the gate oxide film of the 5th and 6th transistors can be found in, *e.g.*, page 18, lines 4 – 8.

Dependent Claim 10

With respect to dependent claim 10, which depends from claim 9, the claim further specifies the first potential level is a positive voltage level and the second potential level is a negative voltage level, as disclosed in original claim 8, which is part of the invention disclosure.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Claims 1 – 6 stand rejected under 35 U.S.C. §112, 1st paragraph, based on the allegation that the specification is non-enabling for the claimed subject matter.

B. Claims 1 – 10 stand rejected under 35 U.S.C. §112, 2nd paragraph, based on the allegation that the claims are indefinite for failing to particularly point out and distinctly claim subject matter which Appellant regards as the invention.

C. The specification stands objected to as containing informalities.

VII. ARGUMENTS

A. The Specification Fully Enables The Subject Matter Of Claims 1 – 6

In the rejection of claims 1 – 6 under 35 U.S.C. § 112, first paragraph, as allegedly failing to comply with the enablement requirement, the Examiner asserts that the claims contain subject matter that was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention because the specification, while being enabling for a level shift circuit, does not reasonably provide enablement for a substrate voltage generating circuit. The Examiner further asserts that, although the Appellants' own Fig. 1 is identified as a "substrate voltage generating circuit" that apparently generates substrate voltage VBB at its output terminal, the figure and disclosure do not clearly show/disclose how this is actually accomplished. Further, the Examiner asserts that the use of "substrate voltage generating circuit" in the preamble of claim 1 does not accurately identify the circuit being described in

the claim. This rejection is traversed, as the Examiner has failed to establish a *prima facie* case with respect to enablement under Sections 112, first paragraph, for the following reasons:

The enablement requirement refers to the requirement of 35 U.S.C. § 112, first paragraph, that the specification describe how to make and how to use the invention being claimed. The Supreme Court decision *Mineral Separation v. Hyde*, 242 U.S. 261, 270 (1916) set forth the test for enablement as: "is the experimentation needed to practice the invention undue or unreasonable?" *In re Wands*, 858 F.2d 731, 737, 8 U.S.P.Q.2d 1400, 1404 (Fed. Cir. 1988) confirms this is still the standard. See also MPEP § 2164.01. In this instance, it is not clear that any experimentation, much less undue experimentation would be required. As identified in MPEP § 2164.01(a), the undue experimentation factors include, but are not limited to:

(a) the breadth of the claims;

(b) the nature of the invention;

(c) the state of the prior art;

(d) the level of one of ordinary skill in the art;

(e) the level of predictability in the art;

(f) the amount of direction provided by the inventor;

(g) the existence of working examples; and

(h) the quality of experimentation used to make or use the invention based on the content of the disclosure.

None of these factors have been addressed by the Examiner in connection with undue experimentation. Insofar as the initial burden rests on the Examiner to provide reasons for lack of enablement, and the Examiner has provided no explanation regarding any of these factors, it is respectfully submitted that this rejection cannot stand, as the record does not establish a *prima facie* case of lack of enablement. *In re Wright*, 999 F.2d 1557, 1562, 27 USPQ2d 1510, 1513 (Fed. Cir. 1993).

As noted in MPEP § 2164.01(a), a conclusion of lack of enablement means that, based on the evidence regarding each of the above factors of the specification, at the time the

application was filed, the specification would not have taught one skilled in the art how to make and/or use the full scope of the claimed invention without undue experimentation. It is not evident that any experimentation need be done to carry out the claimed subject matter, let alone undue experimentation. As such, the rejection is improper and should be withdrawn.

Further to the arguments set forth above, responsive to the Examiner's questioning of how the claimed invention works, Appellants have explained how VBB is generated in the Amendment After Final filed May 30, 2006 that appears to not have been entered by the Examiner.

In the specification, the description of how the presently claimed invention operates in generating VBB (*i.e.*, V_{BB}) in reference to the first power supply voltage VDD (*i.e.*, V_{DD}) and second power supply voltage VSS (*i.e.*, V_{SS}) is provided. For example, beginning on page 11, line 8, the description of how the operation of the substrate voltage generating circuit according to a first embodiment, as shown in Figs. 1 and 2, is discussed. In another example, starting on page 18, line 13, the description of how the presently claimed invention according to a second embodiment, as shown in Figs. 1 and 3, is discussed.

As shown in Fig. 1, for example, the potential level inputs and outputs of each component are clearly shown. For example, NAND 1 can have either VDD or VSS as an output voltage level, output out.101 of level shift circuit 101 can have either VDD or VBB as an output voltage level, and so on. Hence, the behavior of each element in response to a certain input is clearly shown from the input signal OSC/OSC and pump, power supply input VDD and VSS, to the final output signal OUT.vbb with substrate voltage VBB (*i.e.*, V_{BB}).

Appellants note that the output substrate voltage VBB generated is also used as an input to the source of the 5th and 6th transistors N3 and N4, respectively, in Fig. 2. Also, VBB is used as an input voltage at the source of the 5th and 6th transistors N33 and N34, respectively, as shown in Fig. 3. This feedback of the generated VBB substrate voltage, although not explicitly described in the specification, is clearly shown in Fig. 1 with a connection of OUT.vbb to level shift circuits 101 and 102.

Further, VBB at OUT.vbb is generated by making the voltage of capacitor C1 or C2 descend from VSS. Additionally, SW1 and SW2 are switched on alternately. Thus, pulled down voltage VBB is applied to the output node OUT.vbb before the voltage at the output node becoming VSS.

In other words, with respect to the Examiner's assertion that VBB is VSS at the output node OUT.vbb because n1 and n2 are directly coupled to VSS, Appellants respectfully submit that one of ordinary skill in the art would understand that c1 at node n1 and c2 at node n2, as well as VSS, affect voltage VBB at the output node OUT.vbb. Hence, it would be erroneous to conclude that VBB is VSS at the output node OUT.vbb because n1 and n2 are directly coupled to VSS as contended by the Examiner.

In response to the Examiner's assertion that the use of "substrate voltage generating circuit" in the preamble of claim 1 does not accurately identify the circuit being described in the claim, Appellants respectfully submit that claims 1-6 are of varying scopes, with claim 1 being the broadest. That is, claims 1 – 6 are directed to the broadest invention of a substrate voltage generating circuit, with claims 2 and 3 further narrowing the scope by further reciting the details of the level shift circuit of claim 1. Hence, the language in the preamble of claim 1 is proper.

In addition to the arguments set forth above, Appellants respectfully submit that the presently claimed invention is directed to a substrate generating circuit having a level shift circuit and providing a third potential (VBB) level at an output node, as recited in claim 1 which is the broadest claim in the group of claims 1-6. The claimed invention is further narrowed in scope by the additional recital of the structural and functional details of the level shift circuit in dependent claims 2-6, for example.

Cases have held that "if a claim adequately defines patentable subject matter and meets the disclosure and clarity standards of Section 112, then it is proper, even though it may encompass less than what the invention could claim." *Andrew Corp. v. Gabriel Electronics, Inc.* (Fed. Cir. 1988). Further, Applicants respectfully direct the Examiner to MPEP §2164.08 (page 2100-191, Rev. 1, Feb. 2003). It is stated therein that when analyzing the enabled scope of a claim, the teaching in the specification must not be ignored because claims are to be given their broadest reasonable interpretation that is consistent with the specification, and that claims are interpreted in light of the specification does not mean that everything in the specification must be read into the claims. Moreover, according to MPEP 608.01(m), claims should be arranged in order of scope so that the first claim presented is the least restrictive. Keeping in mind of the guideline from the MPEP and legal precedents noted above, Applicants note that claims 1 – 6 are of varying scope, as Applicants' are entitled to claiming, and that independent claim 1 and its dependent claims 2 – 6 do not stand or fall together.

It is respectfully submitted that the Examiner's perception of lack of clarity as alleged in the Office Action is not pertinent to a finding of undue or unreasonable experimentation, which is the test of enablement.

For at least these reasons, the rejection under Section 112, first paragraph should be reversed.

B. Claims 1 – 10 Recite Definite Subject Matter

In the rejection, the Examiner again alleges that there is a lack of clarity as to how the "output node having a third potential level lower than the second potential level" actually relates to the output node being connected to the second power supply node, which is supplied with the "second potential level". Further, the Examiner contends that Appellants' use of "an input signal having the first and second potential levels" in claim 1 (line 8), and the use of "the input signal" in claim 2 (lines 3-6) are confusing. Still further, the Examiner contends that claim 1 appears to imply that the single output signal alternates between the first and second potential levels, and that in claim 2 the same single input signal is applied to the gate of the first through fourth transistors. The Examiner cited Appellants' own Fig. 2 and its associated disclosure that shows the first/second transistor P1/P2 receive complementary input signals, which are not the same "input signal" as claim 2 implies. The Examiner further states that claim 3 has the same type of problem as claim 2, wherein the first/second transistor do not receive the same "input signal" as the limitations on lines 3-6 imply. Finally, the Examiner contends that both independent claims 7 and 9 have the same "input signal" related problems as claims 2 and 3. That is, the Examiner contends that the first/second transistors do not both actually receive the same "input signal" as lines 2-5 of each of claims 7 and 9 imply.

In response to the rejection, Appellants note that the Examiner appears to assume again that the output node would be at the second voltage potential (*i.e.*, VSS) and not at the third voltage potential (*i.e.*, VBB) when SW1 or SW2 are switched on. As noted above, this assumption is not accurate, as SW1 and SW2 switch on alternately and cooperate via feedback with the rest of the level shifting circuits to produce VBB and not VSS.

With respect to the Examiner's confusion between "an input signal having the first and second potential levels" in claim 1 and the use of "the input signal" in claim 2, Appellants note that the features of claim 2 are supported by Fig. 2. As explained in the

previously submitted Amendment, the input signal having the first and second potential levels correspond to VDD and VSS, respectively. In Fig. 1, the input signal are inputted into in.101 of first transistor P1 and /in.101 of second transistor P2. The input signal may take a potential level of H or L (*i.e.*, VDD or VSS, respectively). That is, the input signal to the first transistor P1 is complementary to the input signal transistor P2 as shown in Fig. 2, and the input signal to level shift circuit 101 shown in Fig. 1 are from the output of NAND1 is shown as DSS/VSS and INV 7 as VDD/VSS. Hence, there is no confusion between "an input signal having the first and second potential levels" in claim 1 and the use of "the input signal" in claim 2 as alleged by the Examiner.

With respect to the Examiner's allegation that claim 3 has the same problem as claim 2, Appellants note that the features of claim 3 are supported by Fig. 3, for example. Appellants' clarification of the claim language in claim 2 above and the response to the §112, 2nd paragraph rejection in the Amendment filed September 12, 2005 are also applicable to claim 3. The language "the input signal" directed to the first transistor and the second transistor in claim 3 means that the input signal to the first transistor P31 or to the second transistor P32 may be VDD or VSS (*i.e.*, first and second potential levels, respectively). Due to the complementary nature of the input signal to the first transistor P31 and to second transistor P32, wherein the input signal's may be of VDD and VSS potential level (*i.e.*, first potential level is High and second potential level is Low) as indicated in claim 1, the language "the input signal" in claim 3 is intended to cover the changing nature of the input signal and is deemed as sufficiently clear.

The explanations offered above in relation to the rejection of claims 2 and 3 are also applicable to the rejection of independent claims 7 and 9 and their respective dependent claims 8 and 10. Appellants note that independent claims 7 and 9 do not stand or fall together with their respective dependent claims 8 and 10.

As instructed in §2173.02 of the MPEP, definiteness of claim language must be analyzed, not in a vacuum, but in light of:

(a) The content of the particular application disclosure;

(b) The teachings of the prior art; and

(c) The claim interpretation that would be given by one possessing the ordinary level of skill in the pertinent art at the time the invention was made.

As pointed out above, it is axiomatic that claims are not to be read in a vacuum, but rather in light of Appellants' disclosure and interpretation that would be given by one possessing the ordinary level of skill in the pertinent art at the time the invention was made. By the description in the specification and Appellants' explanations provided thus far, there is no lack of clarity in any of the claimed features.

For at least these reasons, the rejection under Section 112, second paragraph should be reversed.

C. The Specification Does Not Contain Informalities

The abstract of the disclosure is still objected to because, like the title, the abstract is believed to be describing a substrate voltage generating circuit that is not clearly shown or disclosed, with respect to being able to generate voltage VBB. Further, the Examiner asserted that the output signal VBB cannot have a third potential while specifying that the output signal can have a first and a third potential, as disclosed in the abstract of the disclosure. Still further, the Examiner is not clear whether what is meant in the phrase "in response to the output signal VBB" on line 10 of the abstract. Still further, the specification stand objected to as the Examiner is unclear how substrate VBB is transferred to output node OUT.vbb as described on page 13, lines 14 – 17 of the specification, and where does VBB actually come from.

In response to the objection to the specification and abstract, Appellants respectfully note that the level shift circuit outputs VDD (*i.e.*, a first potential) and VBB (*i.e.*, third potential level), as shown in Fig. 1 with the level shift circuit 101 and 102. The output signal of the level shift circuits 101 and 102 is inverted and input into the gate of SW1 and SW2. OUT.vbb, however, outputs VBB. In this regard, Appellants respectfully assert that the specification as well as the abstract contains no unclear language as asserted by the Examiner.

In the objection to the specification, the Examiner appears to also assume that OUT.vbb would be pulled down to VSS (ground) and stays at the ground potential. However, this assumption requires that SW1 or SW2 be switched on and stay on for a period of time until a steady state of 0V is reached at OUT.vbb. Appellants respectfully assert that this assumption is not accurate, as SW1 and SW2 switch on alternately and cooperate via feedback with the rest of the level shifting circuits to produce VBB and not VSS.

VIII. CONCLUSION

For the foregoing reasons, Appellants respectfully submit that the rejections of claims 1 – 6 and claims 1 – 10 under Section 112, 1st and 2nd paragraphs, respectively, and the objection to the specification are unsubstantiated, and thus unsustainable. Accordingly, the rejections are respectfully requested to be reversed.

Respectfully submitted,

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IX. CLAIMS APPENDIX

1. (Previously Presented) A substrate voltage generating circuit comprising:

a first power supply node supplied with a first potential level;

a second power supply node supplied with a second potential level lower than the first potential level;

an output node having a third potential level lower than the second potential level;

a level shift circuit which is coupled between the first power supply node and the output node, which receives an input signal having the first and second potential levels, and which outputs an output signal having the first potential level and the third potential level; and

a switch circuit which connects the second power supply node to the output node in response to the output signal.

2. (Original) The substrate voltage generating circuit according to claim 1, wherein the level shift circuit comprises:

a first transistor of a first conductivity type which has a gate receiving the input signal, a source connected to the first power supply node, and a drain;

a second transistor of the first conductivity type which has a gate receiving the input signal, a source connected to the first power supply node, and a drain coupled to the switch circuit;

a third transistor of a second conductivity type which has a gate connected to the gate of the first transistor, a source, a drain connected to the drain of the first transistor, and a gate oxide film having a first thickness;

a fourth transistor of the second conductivity type which has a gate connected to the gate of the second transistor, a source, a drain connected to the drain of the second transistor, and a gate oxide film having the first thickness;

a fifth transistor of the second conductivity type which has a gate connected to the drain of the second transistor, a source connected to the output node, a drain connected to the

source of the third transistor, and a gate oxide film having a second thickness thinner than the first thickness; and

a sixth transistor of the second conductivity type which has a gate connected to the drain of the first transistor, a source connected to the output node, a drain connected to the source of the fourth transistor, and a gate oxide film having the second thickness.

3. (Previously Presented) The substrate voltage generating circuit according to claim 1, wherein the level shift circuit comprises:

a first transistor of a first conductivity type which has a gate receiving the input signal, a source connected to the first power supply node, and a drain;

a second transistor of the first conductivity type which has a gate receiving the input signal, a source connected to the first power supply node, and a drain coupled to the switch circuit;

a third transistor of a second conductivity type which has a gate connected to the drain of the second transistor, a source, a drain connected to the drain of the first transistor, and a gate oxide film having a first thickness; a fourth transistor of the second conductivity type which has a gate connected to the drain of the first transistor, a source, a drain connected to the drain of the second transistor, and a gate oxide film having the first thickness;

a fifth transistor of the second conductivity type which has a gate connected to the gate of the first transistor, a source connected to the output node, a drain connected to the source of the third transistor, and a gate oxide film having a second thickness thicker than the first thickness; and

a sixth transistor of the second conductivity type which has a gate connected to the gate of the second transistor, a source connected to the output node, a drain connected to the source of the fourth transistor, and a gate oxide film having the second thickness.

4. (Original) The substrate voltage generating circuit according to claim 1, wherein the switch circuit comprises:

a switching element which has a control electrode receiving the output signal, a first electrode connected to the second power supply node, and a second electrode connected to the output node; and

a capacitor coupled between the first electrode and the control electrode.

5. (Original) The substrate voltage generating circuit according to claim 1, wherein the second potential level is 0 volt.

6. (Original) The substrate voltage generating circuit according to claim 1, wherein the third potential level is a negative voltage level.

7. (Original) A voltage level shifting circuit comprising:

a first transistor of a first conductivity type which has a gate receiving an input signal, a source connected to a first supply node supplied with a first potential level, and a drain;

a second transistor of the first conductivity type which has a gate receiving the input signal, a source connected to the first supply node, and a drain coupled to an output node;

a third transistor of a second conductivity type which has a gate connected to the gate of the first transistor, a source, a drain connected to the drain of the first transistor, and a gate oxide film having a first thickness;

a fourth transistor of the second conductivity type which has a gate connected to the gate of the second transistor, a source, a drain connected to the drain of the second transistor, and a gate oxide film having the first thickness;

a fifth transistor of the second conductivity type which has a gate connected to the drain of the second transistor, a source connected to a second supply node supplied with a second potential level lower than the first potential level, a drain connected to the source of the third transistor, and a gate oxide film having a second thickness thinner than the first thickness; and

a sixth transistor of the second conductivity type which has a gate connected to the drain of the first transistor, a source connected to the second supply node, a drain connected to the source of the fourth transistor, and a gate oxide film having the second thickness.

8. (Previously Presented) The voltage level shifting circuit according to claim 7, wherein the first potential level is a positive voltage level and the second potential level is a negative voltage level.

9. (Previously Presented) A voltage level shifting circuit comprising:

a first transistor of a first conductivity type which has a gate receiving an input signal, a source connected to a first supply node supplied with a first potential level, and a drain;

a second transistor of the first conductivity type which has a gate receiving the input signal, a source connected to the first supply node, and a drain coupled to an output node;

a third transistor of a second conductivity type which has a gate connected to the drain of the second transistor, a source, a drain connected to the drain of the first transistor, and a gate oxide film having a first thickness;

a fourth transistor of the second conductivity type which has a gate connected to the drain of the first transistor, a source, a drain connected to the drain of the second transistor, and a gate oxide film having the first thickness;

a fifth transistor of the second conductivity type which has a gate connected to the gate of the first transistor, a source connected to a second supply node supplied with a second potential level lower than the first potential level, a drain connected to the source of the third transistor, and a gate oxide film having a second thickness thicker than the first thickness; and

a sixth transistor of the second conductivity type which has a gate connected to the gate of the second transistor, a source connected to the second supply node, a drain connected to the source of the fourth transistor, and a gate oxide film having the second thickness.

10. (Previously Presented) The voltage level shifting circuit according to claim 9, wherein the first potential level is a positive voltage level and the second potential level is a negative voltage level.

X. EVIDENCE APPENDIX

There are no related evidence to submit at this time.

XI. RELATED PROCEEDINGS APPENDIX

There are no related proceedings to this Appeal.